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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,968	11/21/2003	Gregg Baeckler	15114-093700US	4412
26559 72 AND TOWNSEND AND TOWNSEND AND CREW LLP/ 015114 TWO EMBARCADERO CENTER 8TH FLOOR SAN FRANCISCO, CA 94111-3834			EXAMINER	
			NGO, CHUONG D	
			ART UNIT	PAPER NUMBER
			2193	
			MAIL DATE	DELIVERY MODE
			04/24/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Application No. Applicant(s) 10/718.968 BAECKLER ET AL. Office Action Summary Examiner Art Unit Chuona D. Nao 2193 -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS. WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status 1) Responsive to communication(s) filed on 02 July 2007. 2a) This action is FINAL. 2b) This action is non-final. 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. Disposition of Claims 4) Claim(s) 1-29 and 31-36 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) Claim(s) _____ is/are allowed. 6) Claim(s) 1.3-25 and 27-36 is/are rejected. 7) Claim(s) 2 and 26 is/are objected to. 8) Claim(s) _____ are subject to restriction and/or election requirement. Application Papers 9) The specification is objected to by the Examiner. 10) The drawing(s) filed on is/are; a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abevance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152. Priority under 35 U.S.C. § 119 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. Attachment(s) 1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) Paper No(s)/Mail Date. Notice of Draftsperson's Patent Drawing Review (PTO-948)

Information Disclosure Statement(s) (PTO/S5/08)
 Paper No(s)/Mail Date ______

5) Notice of Informal Patent Application

6) Other:

DETAILED ACTION

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and recuirements of this title.

 Claims 29 and 31-36 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 29 and 31-36 are directed to a computer implemented method of calculation. In order for a claimed invention that is directed to such a computer implemented method of calculation to be statutory, the claimed invention must accomplish a practical application. That is the claimed invention must transform an article or physical object to a different state or thing, or produce a useful, concrete and tangible result. State Street, 149 F.3d at 1373-74, 47 USPQ2d at 1601-02. Also see "Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility", MPEP 2106 and OG Notices: 22 November 2005. It is clear from claims 29 and 31-36 that the claims merely involves calculations and manipulations of data in performing calculations. The claimed invention does not transform an article or physical object to a different state or thing. The inputs are numbers and the outputs are also numbers. The result of the invention is merely a values without a practical application recited in the claims to make the result useful, concrete and tangible. Therefore, the claimed invention is directed to nonstatutory subject matter as the claims fails to assert a practical application to the invention. It should be noted that a part of a total sum or the total sum or a mathematical operation result of binary numbers is a mere number. It does not have any real world value, and thus is not a

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tangible result.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on

sale in this country, more than one year prior to the date of application for patent in the United States.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth as section 102 of this title, if the differences between the subject matter sought to be patented and the prior at are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability skill not be are loss that the subject matter pertains. Patentability skill not be are loss that the subject matter pertains. Patentability skill not be are loss that the subject matter pertains. Patentability skill not be are loss that the subject matter pertains. Patentability skill not be are loss that the subject matter pertains. Patentability skill not be a regatived by the subject matter pertains. Patentability skill not be a regatived by the subject matter pertains. Patentability skill not be regatived by the subject matter pertains.

manner in which the invention was made.

5. Claims 1,3,8-11,16 and 17 are rejected under 35 U.S.C. 102(b) as being clearly

anticipated by Rothman et al. (5,898,602).

As per claims 1,3,8 and 9, Rothman et al. discloses in figure 4 a logic circuit including a

first LUT (10) in a first LE (ALU0) for determining a carry (C1) from a first set of corresponding

bits (A0,B0,C0) of at least three binary numbers (A,B,C), a second LUT (15) in a second LE

(ALU1)) for determining a sum (F1), from a second set (A1.B1) of corresponding bits of the

binary numbers, and an adder (the EXOR gate that outputs S1 and is also a hardwired modulo-2

adder) in the second LE for adding the carry and the sum as claimed. It should be noted that the

claims do not require the second set of corresponding bit of at least three binary numbers, and C

can clearly be viewed as a binary number.

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As per claims 10,11,16 and 17, Rothman et al. discloses in figure 4 a logic element (ALU1) including a hard wired adder (the EXOR gate that outputs S1), and an AND gate that is connected to C1 and that can be viewed as the claimed multiplexer for selecting between a signal determined in the logic element having a value 0 and a signal (C1) determined in a previous logic element for forwarding to the adder, wherein the AND gate corresponding to the claimed multiplexer selects C1 when the LE si set to operate in an addition of three binary numbers (A1,B1,C1) as claimed.

 Claims 10 and 11 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Cohen et al. (5,511,017).

Cohen et al. discloses in figure 6 a logic element (15,17,25 29,33,35) including a hardwire carry save adder (35, see also figures 3 and 4) and a multiplexer (33) for selecting between a signal (output of 17) determined in the logic element and a signal (output of 47) determined in a previous logic element (47,50,62,64,68) for forwarding to the adder as claimed. It should be noted that the adder (35) always perform an addition of three binary number at its three inputs.

 Claims 1,3-9,12-25,27-29 and 31-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen et al. (5.511,017) in view of Rothman et al. (5.898,602).

As per claims1,3-9,12-20,23,24,29 and 31-36 Cohen et al discloses in figure 4 a logic circuit including a first logic element (LE) having a CSA cell (32-0) for producing a carry (C0) from a first set of corresponding bits of at least three binary numbers (X,Y,Z); and a second LE

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having a CSA cell (32-1) for producing a sum (S1) from a second set of corresponding bits of the binary numbers and an hardwired adder (34-1) in the second logic element for adding the carry and the sum as claimed. It is noted that Cohen et al does not discloses the CSA cell in each LE having a first look-up table (LUT) for producing a carry and a second LUT for producing a sum. However, Rothman et al discloses in figures 5 and 6 an implementation of an adder cell (40), which have same function as that of a CSA cell, by programmable logic device having a first LUT (30) and a second LUT (50) for respectively producing a carry and a sum having the same functions as claimed (see also figure 7). It would have been obvious to a person of ordinary skill in the art to implement the CSA cells in Cohen et al. by programmable logic devices having a first LUT (30) for producing a carry and a second LUT (50) for producing a sum as taught by Rothman et al. in order to increase the flexibility of the logic circuit.

As per claims 21,22,25,27 and 28 each claimed LE is viewed as a group of two consecutive CSA cells with two consecutive full adder cells in figure 4 of Cohen et al.

- 8. Claims 2 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- Applicant's amendment necessitated the new ground(s) of rejection presented in this
 Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a).
 Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong D. Ngo whose telephone number is (571) 272-3731. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis, Jr. A. Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chuong D Ngo/ Primary Examiner, Art Unit 2193

04/22/2008